REMARKS

Applicants have amended claim 6 to correct dependency, amended claim 10 to improve English usage, and amended claim 27 to reflect the invention as disclosed.

Applicants confirm the election of the claims of Group I, claims 1-12 and 25-28, as the Examiner properly stated in paragraph 1 of the Action. However, applicants respectfully disagree with the Examiner with respect to the manner in which the requirement was stated and the grounds for the requirement and thus partially traverse the requirement.

The Action of October 8, 2002, was styled as a restriction requirement in paragraph 1 and set forth mutually exclusive groups of claims from which to elect, in accordance with usual practice. Paragraph 2 set forth reasons why the groups of claims identified in paragraph 1 are distinct, but instead referred to "patentably distinct species of the claimed invention," which is the language used in connection with election of species requirements, which are *not* the same as restriction requirements. The Examiner compounded the confusion by referring to claim 1 as generic. In their previous response, applicants pointed out to the Examiner that the Examiner should have given applicants the option of selecting "species" because the Examiner required applicants to elect a single species for prosecution and admitted that claim 1 is a generic claim. In this Action, the Examiner still maintains that this is an election of species requirement without responding to applicants' arguments. Applicants respectfully submit that the Examiner should recognize that he imposed a restriction requirement, which should be withdrawn because claim 1 is a generic claim as the Examiner concedes, leading to the result that all of the claims are directed to the same invention regardless of the classification of various claims in various classes of art.

Applicants attach a new declaration as required in paragraph 2 of the Action.

Claims 6, 9 and 10 have been rejected under 35 USC 112, second paragraph as indefinite. The Examiner contends that "the resistor" of claim 6 lacks antecedent basis, "the first and second connections" of claim 9 lack antecedent basis, and "portions of the first and second transistors" and "portions of the third and fourth transistors" of claim 10 are unclear.

Claim 6 as amended includes "the resistor", which finds antecedent basis in "a resistor" of claim 5. The first connection of claim 9 finds antecedent basis in "a first connection" of claim 4, and the second connection of claim 9 finds antecedent basis in "a second connection" of claim 7. Claim 10 as amended clearly defines the configuration of the transistors with respect to the corresponding input terminals. Accordingly, this rejection should be withdrawn.

Claims 25 and 27 have been rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 6,124,736 (Yamashita). Applicants respectfully traverse this rejection.

Claim 25 is directed to a semiconductor device which is the combination of a first switch and a second switch. The first switch has two field-effect transistors and a common output terminal pad for the two transistors of the first switch. Each of the transistors has a source electrode, a gate electrode, a drain electrode and an input terminal pad. The source electrode or the drain electrode of each of the two transistors is connected to the common output terminal pad, and the source electrode or the drain electrode of each of the two transistors which is not connected to the common output terminal pad is connected to the input terminal pad. As a result, one of the signals inputted to the two input terminal pads is outputted from the common output terminal pad because the common output terminal pad is connected to the source or drain of each of the transistors. The second switch of claim 25 has the same features as the first switch.

The Examiner contends that the logic circuit C200 shown in FIG. 3 of Yamashita corresponds to the switching device of claim 25, including the feature that the common output terminal is connected to the source or drain of each of the transistors. The Examiner cites one of

the leads that carries an output signal O' as the common output terminal pad of claim 25. However, the lead for the output signal O' of Yamashita is not the common output terminal pad of claim 25. First, Yamashita does not describe a discrete device that needs terminal pads for external connection. Nowhere in Yamashita is a device having terminals pads described. In the absence of such a description, persons of ordinary skill in the art would have understood that the logic circuit C200 is a part of larger circuitry and is not a discrete device that requires terminal pads for external connection. Second, the lead for the output signal O' of Yamashita is not connected to the source or drain of each of the transistors. The first switch of Yamashita's logic circuit does have two transistors T200, T201 that have a source and drain, respectively. However, neither the source or the drain of each of the transistors T200, T201 of Yamashita is connected to the lead for the output signal O'. Instead, the source or drain, which is not connected to the lead for input signals I0, I0', is connected to a gate of other transistors T206, T207. Accordingly, the signals I0, I0' inputted to the leads for signal input are not outputted from the lead for the output signal O' because the lead for the output signal O' is not connected to the source or drain of the transistors T200, T201. Yamashita thus does not teach or suggest the feature of the common output terminal pad of claim 25.

Claim 27 as amended recites two single pole double throw switches and the feature that each of the two switches receives two high frequency signals through two of the four input terminals and outputs one of the two high frequency signals to one of the two common output terminals in response to a control signal received from one of the control terminals. This amendment finds support, for example, on page 6, line 26 - page 7, line 21. As explained above, Yamashita's logic circuit does not describe any terminal pad as a part of its device structure or the feature that the signal entering the device at the input terminal pads comes out of the device at the common output terminal pad. In addition, Yamashita's device is a logic circuit that

manipulates signals of "1" and "0." See, for example, FIG. 1 and the related description in column 14, lines 55-65 of Yamashita. Yamashita's device is not configured to switch high frequency signals, such as CDMA and GPS signals, as is the case with the switching device of claim 27. Accordingly, Yamashita does not teach or suggest the feature of claim 27.

Thus, the rejection of claims 25 and 27 should be withdrawn.

Claims 1-5, 7, 8, 10-12, 26 and 28 have been rejected under 35 USC 103(a) as being unpatentable over Yamashita in view of the description of the prior art in the specification. Applicants respectfully traverse this rejection.

Claim 1 includes the same feature as claim 25 that the common input terminal pad is connected to the source or the drain of the corresponding transistors. As explained above, Yamashita does not teach or suggest this feature of claim 1. Accordingly, Yamashita and the prior art description of the specification do not teach or suggest the switching device of claim 1 as a whole.

Furthermore, applicants point out to the Examiner that without specific suggestion or motivation persons skilled in the art would have not combined the Yamashita's device and the prior art description of the specification to produce the switching device of claim 1 because Yamashita describes a logic circuit that manipulates signals of "1" and "0" and the switching device of claim 1 switches high frequency signals. Most notably, Yamashita's device is best suited for silicon-based devices and the switching device of claim 1 is best suited for compound-semiconductor based devices. The Examiner provides no reference to any portion of Yamashita or the specification that provides such a suggestion or motivation.

Applicants further point out to the Examiner that Yamashita describes only abstract circuit designs and does not describe claimed device structures. All the drawings and the related descriptions of Yamashita only provide circuit diagrams. The switching device of this invention

achieves a more compact design of the switching device. See page 20 ,lines 4-15, of the specification. To achieve a compact design of the switching device, applicants not only provide a suitable circuit design but also provide the device structures in a wiring layout level. Those structures are clearly recited in the claims. For example, claims 4 and 5 include the configuration of the connection, or the resistor, with respect to the transistors, claim 7 includes the configuration of the two connections, claim 8 includes the configuration of the terminal pads in the device, and claim 10 includes the configuration of the transistors with respect to the terminal pads. Yamashita does not describe these devise structures in the wiring layout level recited in the claims.

Thus the rejection of claims 1-5, 7, 8, 10-12, 26 and 28 should be withdrawn.

In light of the above, a Notice of Allowance is solicited.

Attached hereto is a marked-up version of the changes made to the claims by this amendment, captioned "**Version with markings to show changes made**".

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. **492322002400**.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Amend claims 6, 10 and 27 as follows:

6. (Amended) The semiconductor switching circuit device of claim [4]5, wherein the substrate is made of a compound semiconductor and the resistor comprises a high dopant concentration region.

10. (Amended) The semiconductor switching circuit device of claim 8, wherein [portions] a portion of the first transistor and a portion of the second [transistors] transistor are disposed between the first and second input terminal pads, and wherein [portions] a portion of the third transistor and a portion of the fourth [transistors] transistor are disposed between the third and fourth input terminal pads.

27. (Amended) A semiconductor switching circuit device comprising:

four input terminal pads;

two common output terminal pads; [and]

no more than two control terminal pads; and

two single pole double throw switches, each of the switches receiving two high frequency signals through two of the four input terminals and outputting one of the two high frequency signals to one of the two common output terminals in response to a control signal received from one of the control terminals.